NIST

National Institute of Standards and Technology

Technology Administration

U.S. Department of Commerce

NISTIR 6707

January 2001

Electronics and Electrical Engineering Laboratory

Office of Microelectronics Programs

Programs, Activities, and Accomplishments

The National Semiconductor Metrology Program

1901-2001 ENNIAL

The Electronics and Electrical Engineering Laboratory

Through its technical laboratory research programs, the Electronics and Electrical Engineering Laboratory (EEEL) supports the U.S. electronics industry, its suppliers, and its customers by providing measurement technology needed to maintain and improve their competitive position. EEEL also provides support to the federal government as needed to improve efficiency in technical operations, and cooperates with academia in the development and use of measurement methods and scientific data.

EEEL consists of five programmatic divisions, two matrix-managed offices, and a special unit concerned with magnetic metrology:

- Electricity Division
- Semiconductor Electronics Division
- Radio Frequency Technology Division
- Electromagnetic Technology Division
- Optoelectronics Division
- Office of Microelectronics Programs
- Office of Law Enforcement Standards
- Magnetics Group

This document describes the technical programs of the Office of Microelectronics Programs. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220,
On the Web: www.eeel.nist.gov

Cover Caption: The National Semiconductor Metrology Program (NSMP) is a NIST-wide effort desigend to meet the hightest priority measurement needs of the semiconductor manufaturing industry and its supporting infrastructure needs of the semicondutor manufacturing industry and its supporting infrastructure industries. Research efforts include clean room technology as it pertains to particle contamination and contamination free manufatturing; rapid thermal processing (RTP) as shown in the RTP Thermometry Test Bed Chamber for developing more accurate wafer temperature measurement; and Nanometer-Scale Diminsional Metrolgoy with Atomic Force Microscopy-a Calibrated Atomic Force Microscope image of a specimen and tap lines on a SOI linewidth specimen. The line is ~500 nm wide.

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U.S. DEPARTMENT OF COMMERCE
Donald L. Evans, Secretary

Technology Administration
Karen H. Brown, Acting Under Secretary for Technology

National Institute of Standards and Technology
Karen H. Brown, Acting Director

Disclaimer: Certain commercial equipment and/or software are identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 1999. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Appendices: An index of researchers associated with the NIST-wide projects is located in Appendix A. Appendix B contains a listing of all projects by Operating Unit. Appendix C is a key to funding source acronyms.

Contents

Welcome

The **Office of Microelectronics Programs** provides coordination of silicon semiconductor manufacturing metrology activities across NIST to maximize the impact of this critical industry on the health of the U.S. economy. The Office, with a permanent staff of three, is located in Gaithersburg, Maryland, and is one of the two Offices in the Electronics and Electrical Engineering Laboratory at NIST.

Many of the projects managed by the Office are cooperative activities across several Operating Units. Thus the projects are able to leverage the best expertise available for the specific task across NIST, regardless of organizational structure. Our projects are also aligned by research TASK area: Critical Dimension and Overlay; Two- and Three-Dimensional Dopant Profiling; Thin Film and Defect Characterization; Interconnect and Packaging; Lithography; and Modeling, Design and Test.

- Additional activites of the Office which insure timely response to industry needs include:
- Extensive interactions with industry consortia, such as the Semiconductor Research Corporation (SRC) and International SEMATECH (ISMT).
- Participation in the roadmapping activities commissioned by the Semiconductor Industry Association and administered by International SEMATECH.
- Standards bodies activities related to the semiconductor industry including the Semiconductor Equipment and Materials International (SEMI) standards program, American Society for Testing of Materials (ASTM) in the US, and Deutsches Institut fur Normung (DIN) in Germany.

For additional information about the Office of Microelectronics Programs, please visit our web site http://www.eeel.nist.gov/omp/

Vision

The **Office of Microelectronics Programs** will be recognized as an outstanding organization managing and coordinating projects key to meeting the metrology needs of the semiconductor manufacturing industry.

Values

The **Office of Microelectronics Programs** values relevance and focus of its projects in solving crucial metrology issues facing the semiconductor manufacturing industry. The Office values the technical excellence and the dedication of the scientists, engineers, and technicians participating in the National Semiconductor Metrology Program.

Mission

The mission of the **Office of Microelectronics Programs** is to manage the National Semiconductor Metrology Program (NSMP), a NIST-wide effort designed to meet the highest priority measurement needs of the semiconductor manufacturing industry and its supporting infrastructure industries as expressed by the International Technology Roadmap for Semiconductors and other authoritative industry sources. The NSMP was established in 1994 with a strong focus on mainstream silicon CMOS technology and an ultimate funding goal of $25M. It is currently at $12M, with a broad portfolio of semiconductor metrology development projects conducted in six of the Operating Units of the Measurements and Standards Laboratories of NIST:

- Electronics and Electrical Engineering Laboratory (EEEL)
- Manufacturing Engineering Laboratory (MEL)
- Chemical Sciences and Technology Laboratory (CSTL)
- Physics Laboratory (PL)
- Materials Science and Engineering Laboratory (MSEL)
- Building and Fire Research Laboratory (BFRL)

Goals

The Office of Microelectronics Programs will:

- Diligently identify critical metrology gaps confronting the semiconductor manufacturing industry, and implement robust projects to confront those needs;
- Insure expeditious technology transfer of NSMP results to the industry; and
- Assist the NIST technical body in interfacing efficiently with key elements of the semiconductor manufacturing industry and its research and development community.

Office of Microelectronics Programs Organization

(810.01)

2871 KNIGHT, Stephen, Director

4400 BUCKLEY, Michelle, Secretary

8125 MARTINEZ DE PINILLOS, Joaquin, V.,

Senior Scientist

5198 SCACE, Robert I. (GR/CTR)

2248 BELZER, Barbara J., Technical Staff Assistant (PT)

Legend:

CTR = Contractor
GL = Group Leader
GR = Guest Researcher
PD = Postdoctural
Appointment
PL = Project Leader
PT = Part Time
S = Student
ACT= Acting

Telphone numbers are:
(301) 975-XXXX, (the four
digit extension as indicated)

Permanent staff can generally
be contacted by email using
the following format:
firstname.lastname@nist.gov

Critical Dimension and Overlay

Task Goals

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. Lithography currently constitutes ~35% of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, and critical comparisons of different critical dimension and overlay measurement techniques.

Customer Needs

The 1999 International Technology Roadmap for Semiconductors (ITRS) cites in Table 38 that the five difficult challenges for the >100 nm node (pre-2005) include resolution enhancement techniques and post optical technique mask fabrication, consensus among manufacturers for the technology used, development of processes to control minimum feature size to less than 7 nm, 3 sigma and development of new and improved alignment and overlay control methods independent of technology options. For the technology nodes < 100 nm, development of mask process control methods is required to achieve critical dimension, image placement, and defect density acceptable in this regime. Also necessary are the development of processes to control minimum feature size to < 5 nm, 3 sigma and the development of new alignment and overlay control methods independent of technology options. Currently, resolution improvements have outpaced overlay and CD measurement improvements. It is believed that to keep costs reasonable and production high, a total system approach must be employed.

The industry needs to arrive at a consensus regarding the measurement technology that will be used as the geometries continue to shrink. Reference materials traceable to NIST as well as standards measurement methodology need to be developed which address the continuing needs of the industry.

Technical Strategy

Reference materials traceable to NIST and standard measurement methodologies require that NIST develop a clear understanding of the uncertainties associated with in-line critical dimension measurements. Evidence exists that by combining the strengths of SEM (excellent lateral information) and SPM (excellent height information), a significant reduction in measurement uncertainties can be achieved.

Development of a metrology such as a calibrated Atomic Force Microscope (AFM) and devising both a calibration service and a Standard Reference Material (SRM) will support tool matching requirements in industry fabrication facilities.

NIST continues to work toward ensuring fully automatic size and shape measurements of 3-dimensional features ≤ 180 nm that are completed in seconds with an accuracy and precision approaching atomic levels. Collaborative and cooperative interactions with industrial partners, both domestic and international, will assist reaching these goals and establishing traceability to NIST.

Projects

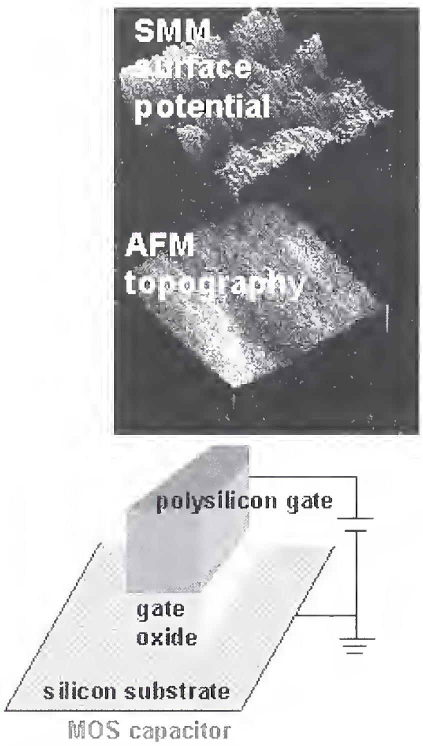
Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques

OU: MEL

Researchers: John Dagata, Michael Postek

Funding Sources: NIST OMP (50%), Other Agency (50%)

- Improve measurement uncertainty of SEM CD measurements by modeling of intensity profiles required to obtain reliable estimates of step heights;
- Utilize the NIST built combined SEM and SPM instrument to test the feasibility of a two-method approach;
- Partner with a university to develop software permitting 3-D image reconstruction.



Comparison of the topographical and electrical homogeneity of a polysilicon gate using atomic force microscopy (AFM) and Scanning Maxwell-Stress Microscopy (SMM)

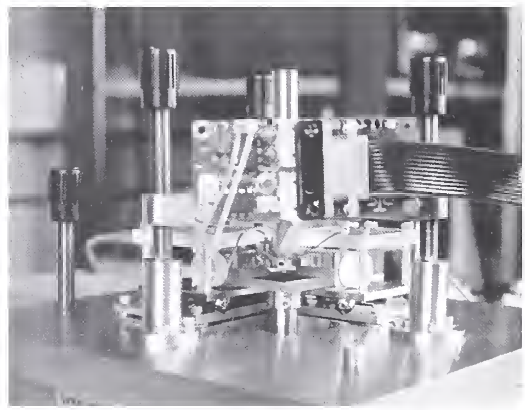
Nanometer-Scale Dimensional Metrology and Atomic Force Microscopy

OU: MEL

Researchers: Ronald G. Dixon, Theodore Vorburger

Funding Sources: NIST OMP (26%), NIST STRS (51%), NIST ATP (15%), Other Agency (8%)

- Develop of Calibrated AFM (C-AFM) designed to aid the development of AFM standards;
- Conduct an industrial round robin and improve uncertainty levels of 1.5 nm at the sub-micron level;
- Continue development of SRM 2089 for release in 2002.



Calibrated AFM

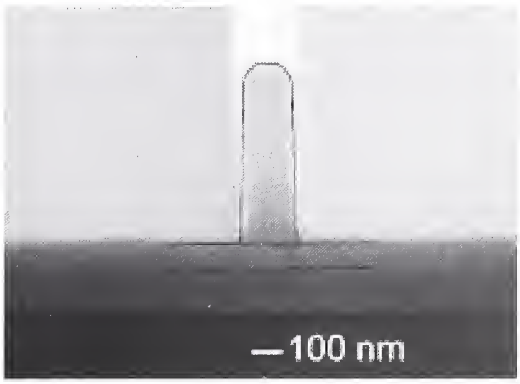
Scanning Electron Microscope Dimensional Metrology

OU: MEL

Researchers: Michael Postek

Funding Sources: NIST OMP (25%)
Other Agency (75%)

- Develop standard artifacts for processes at 150 nm and below;
- Issue SRM 2091;
- Evaluate procedure for correctly measuring image sharpness collaboratively with International SEMATECH.



Cross-sectional view of a resist line overlaid with the structure calculated from top-down view of the line by Adaptive Monte Carlo Modeling

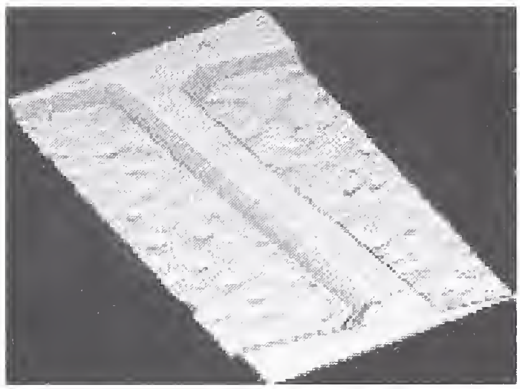
Model-Based Linewidth Metrology

OU: MEL

Researchers: John S. Villarrubia
Andras Vladár
Michael Postek

Funding Sources: NIST OMP (50%)
Other Agency (50%)

- Cooperative interaction among practitioners of various techniques sharing information with the goal of improving linewidth measurement capabilities within NIST and the Semiconductor Industry;
- Develop competence sufficient to calibrate an industrially relevant wafer linewidth standard;
- Transfer improved measurement methodology developed at NIST to industry



Atomic force microscope image of a single crystal critical dimension artifact

Linewidth Standards for Nanometer Metrology

OU: EEEL

Researchers: Michael W. Cresswell
Richard A. Allen

Funding Sources: NIST OMP (99%)
Other Agency (1%)

- Develop test-structure-based electrical metrology methods and related reference materials that have the primary emphasis on linewidth metrology and calibration.

- Develop a traceability pathway for dimensional certification provided by HRTEM imaging and a secondary reference using sub-nanometer repeatability of electrical CD metrology.

Lattice-plane selective etches provide reference features with atomically planar sidewalls

Atom-Based Dimensional Metrology

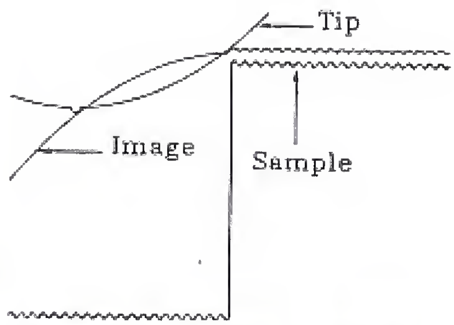
OU: MEL

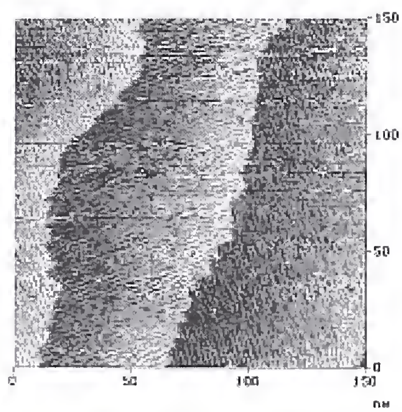
Researchers: Richard M. Silver

Funding Sources: NIST OMP (20%)
NIST STRS (25%)
Other Agency (55%)

- Develop 3-Dimensional structures of controlled geometry whose dimensions can be traced directly to intrinsic crystal lattice;

- Develop methods to prepare photolithographically patterned 3-D structures in Si and GaAs. Structures must be prepared in such materials as to allow the atomic surface reconstruction of those features such that the atomic order is commensurate with the underlying crystal lattice. This fabrication is to occur at International SEMATECH.





Vacuum atomic force microscope image of lattice steps in silicon

Optical Overlay and CD Metrology

OU: MEL

Researchers: James Potzick
Richard Silver

Funding Sources: NIST OMP (50%)
Other Agency (50%)

- Develop instrumentation and overlay metrology methodology for optical overlay CD measurements;
- Design and calibrate standard artifacts for optical overlay and CD metrology;
- Develop microlithography process modeling for the improvement of photomask metrology to improve its effectiveness through exposure emulation, making the needed tools readily available to customers and easy to use;
- Develop an open framework for snap-together microlithography process simulation products from diverse suppliers, which together model the specifications-to-wafer process;
- Simulate, under intended exposure and development conditions, photomask performance based mask design and on mask measurements;
- Link existing and new simulation products through dialog and consensus among a group of leading suppliers and users of process modeling software and related metrology tools.

High Accuracy Two-Dimensional Metrology

OU: MEL

Researchers: Ted Doiron
Richard Silver

Funding Sources: NIST OMP (100%)

- Develop an artifact standard that can be used to bring all the 2-Dimensional based inspection instruments to the same metric;
- Develop an industry consensus standard grid, measure by the state-of-the-art measuring machines in private industry, and verify the measurements using NIST capabilities;
- Develop an artifact standard that can be used to bring all the 2-D based inspection instruments to the same metric.

Significant Accomplishments

- In cooperation with a researcher at the University of Tennessee-Knoxville, we have demonstrated that nano-tips used in high-resolution scanning electron microscopes can significantly improve the signal to noise over results achievable with conventional field emission tips.

- A process has been developed that allows for renewal of nano-tips for field emission electron guns used in ultra-high resolution scanning electron microscopy.

- In the course of measuring linewidth on single-crystal artifacts, researchers have determined that SEMs have extraordinary sensitivity to tilt. This allows the development of highly reproducible orientation references, for example, on an SEM's sample positioning stage.

- New image recognition and quantitative image analysis software has been developed which allows the evaluation of numerous effects on algorithm performance to quantify feature roughness and asymmetry effects on an overlay pattern. The code has been used extensively to evaluate and compare several cross-correlation, auto-correlation, and new least-squares correlation methods.

- A silicon-wafer carrier has been developed that mimics the appearance of a product wafer to metrology systems. The artifact incorporates exact orthogonality of the recessed pit containing the test chip, flatness of the pit floor, control of the lateral dimensions of the pit, and pit sidewall slopes crystallographically defined at 54.37 degrees. Technology transfer to a commercial collaborator has resulted in the production of a prototype in wafer sizes commensurate with current manufacturing capabilities.

- The process collaboratively developed at Sandia National Laboratories by NIST and Sandia researchers that has been used to make the prototype single-crystal CD reference materials is being transferred to VLSI Standards, Inc. VLSI Standards is evaluating the prospects of producing CD reference materials based on this technology.

- The work of the Semiconductor and Materials International (SEMI) Standards task force on metrology terms and definitions has become the industry standards SEMI P35-0200, "Terminology for Microlithography Metrology." To coordinate semiconductor metrology terms with usage in other industries, this standard contains definitions from the International Organization for Standardization (ISO) "International Vocabulary of Basic and General Terms in Metrology", reference to the ISO "Guide to the Expression of Uncertainty in Measurement", and terms describing some new concepts in the measurement of microscopic feature size of linewidth.

- developed an instrument in-house, capable of performing concurrent scanned probe microscope- (SPM) based nanolithography, dimensional and electrical characterization by scanning Maxwell-stress microscopy (SMM), and traditional device probing has been demonstrated using a silicon lateral-tunneling Silicon On Insulator (SOI) device test structure.

- A NIST researcher, working with collaborators in Japan and Taiwan, has achieved significant improvements in the performance and sensitivity of electric force microscopy for nanoelectronic device characterization.

- NIST and the Physikalish-Technische Bundesanstalt (PTB) completed a set of measurements on a prototype two-dimensional grid. This same plate was measured at several industrial sites as well, and is a critical link in the international traceability chain.

Two- and Three-Dimensional Dopant Profiling

Task Goals

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, complicating both modeling and doping gradient measurements. The overall task of these projects is to provide suitable metrology for this stochastic regime.

Customer Needs

In 1999, the ITRS expresses the desired spatial resolution of 3 nm and precision in concentration of ±5%. By 2005, resolution of 1.5 nm and ± 3% precision in at-line dopant concentration is proposed. Scanning Capacitance Microscopy (SCM) has emerged as a leading contender to provide 2-D carrier profiles. SIMS is most likely to provide the solution to precision requirements for dopant concentration measurements. Relatively accurate profiles of the dopant concentration can by obtained when SCM images are combined with SIMS measurements.

Technical Strategy

At the device dimensions projected, the ability for those devices to work depends strongly on the carrier concentrations throughout the material. It is therefore essential that techniques and methodologies are developed which can support these needs and that reference materials and standards are made available for calibration of the in-line tools.

The two projects in this area share a goal to develop physical models based on their research results and proved interpretation formalisms for the images and measurements obtained.

Researchers are developing depth profiling reference materials and reference materials for Scanning Capacitance Microscopes (SCMs) in addition to providing 2-D carrier profiles using SCM and developing 3-D physical models. There is also significant development in devising measurement methodologies for the depth profiling techniques using Secondary Ion Mass Spectrometry (SIMS) with ion sources unique to NIST.

Projects

Scanning-Probe Microscope Metrology

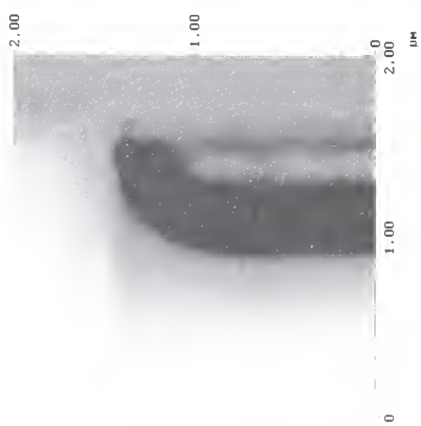
OU: EEEL

Researchers: Joseph J. Kopanksi
Brian G. Rennex
Jay. F. Marchiando

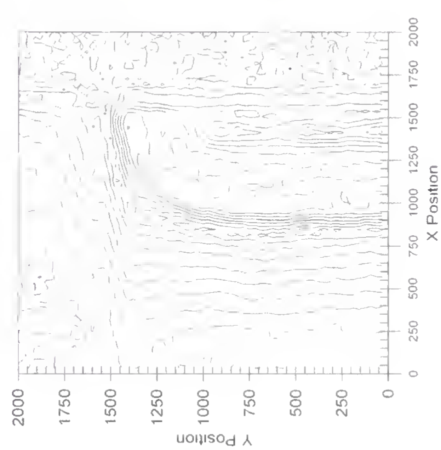
Funding Sources: NIST OMP (100%)

- Develop measurement methodology, physically based models, and interpretation formalisms to make Scanning Capacitance Microscopy a practical metrology for 2-D carrier profiling of silicon;

- Develop 2-D and 3-D finite element solutions of Poisson's equation for the SCM geometry and transfer this capability to industry through NIST developed software, FASTC2D.



SCM image of a p+1n junction



Dopant contours extracted with FASTC2D

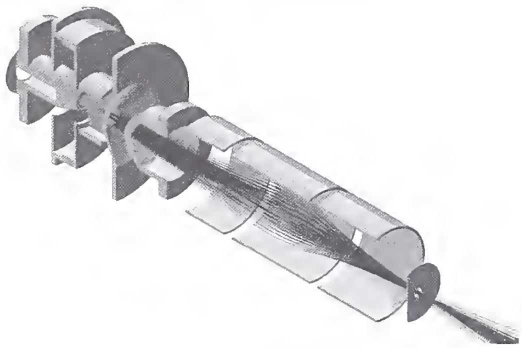
Thin-Film Profile Measurement Methods and Reference Materials

OU: CSTL

Researchers: David S. Simons
Greg Gillen

Funding Sources: NIST OMP (100%)

- Improve the capabilities for compositional depth profiling to support the semiconductor industry;
- Define optimum procedures for ultra-high depth resolution and ultra-shallow profiling by SIMS;
- Develop depth-profiling reference materials needed by the semiconductor industry;
- Develop methods to improve uncertainty of implant dose measurement by SIMS (International SEMATECH collaboration).



Ion Source

Significant Accomplishments

- *FASTC2D* version 1 software code was completed and distributed to the 40-member SEMATECH working group on 2-D profiling. User feedback and comments were incorporated into the code.
- Collaboration began with Los Alamos National Laboratories (LANL) to use their LaGriT (Los Alamos Gridding Toolkit) software as a library of user-callable tools. Jay Marchiando spent a 3-month sabbatical during the summer of 2000 at LANL learning to use and apply LaGriT.
- Interaction initiated with Howard University, Washington, D.C., to apply SCM to high bandgap semiconductors. A senior engineering student has taken on a project to make a preliminary study of SCM in applying it to silicon carbide as her senior project.
- A project was initiated with International SEMATECH (ISMT) to study improved methods for depth profiling of thin ZrO_2 gate dielectric materials. Depth profiles conducted with the NIST prototype SF_5^+ primary ion source demonstrated superior depth resolution and minimal artifacts as compared to SIMS depth profiling with more conventional Cs^+ or O_2^+ primary ion beams.

Thin-Film and Defect Characterization

Task Goals

As device dimensions continue to shrink, critical films approach the realm of several atoms thick, challenging thickness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2, will soon no longer be viable. The overall task is to provide suitable metrology and reference materials for thin dielectrics and conducting barrier films, including electrical characterization, thickness and roughness metrology, and reliability metrology.

Customer Needs

The 1999 ITRS indicates near that in the near term, 2003-2005, equivalent gate dielectric thickness needs to be ~ 1.5 nm with process tolerance of $\pm$ 4% (3 σ). The reliability of SiO_2 at this thickness level is not sufficient. The physics of failure and traditional reliability techniques must be reexamined for ultrathin dielectrics that exhibit excessive tunneling current and soft breakdown. There is a need for refining electrical and reliability characterization methodologies, establishing standard reference data, and developing a fundamental understanding of the relationship between gate dielectric material and device electrical measurement.

Spectroscopic Ellipsometry (SE) is a preferred measurement method for process monitoring, as it is non-invasive, non-destructive, and is relatively quick. In addition to on-line and at-line measurements accurately determining thickness of gate dielectrics, SE is shown to make significant contributions toward the development of techniques to determine the structure of the films and their interfaces. Improvements must be made in the understanding between physical, electrical, and optical determination of film properties. Research is needed to link these methods together and provide models, data, and standards for transferring the information to the industry.

Other research areas are needed that investigate techniques minimizing material dependent calibration requirements for in-line tools. There is currently a comprehensive effort at NIST using x-ray measurement methods.

Future gate dielectrics pose problems in chemical status and layer thickness determination of < 8 nm. A need exists not only for improvements in measurement accuracy and refinement in available measurement technologies, but improvements in the data used to analyze silicon and the dielectrics grown upon it.

Technical Strategy

Seven interrelated and often complementary projects offer a diverse approach to arriving at practical solutions to thin film characterization needs. The pace of development demands creative solutions for devising practical mechanisms for measurements that are traceable to NIST including Standards Reference Materials (SRMs), NIST Traceable Reference Materials (NTRMs), and Standard Reference Data (SRD). We are involved in a collaboration to extend characterization schemes developed on thin oxide and oxide-nitride gate dielectrics to the newer metal oxides and silicate dielectrics.

Much of the characterization is tied to the reliability effort. The physical mechanisms responsible for "soft" or "quasi" breakdown modes in ultra-thin SiO_2 films and its implications for device reliability are being investigated as a function of test conditions and temperature. Tests are used to determine the thermal and electrical acceleration parameters of device breakdown. Our efforts include providing insight to the physical mechanisms of ultra-thin gate oxide wear-out and breakdowns. We are applying electrical measurement techniques, procedures, and analysis.

Determining the electrical and physical properties of thin oxide and alternate gate dielectrics require that we relate optical, electrical, and physical measurements of thickness. Our approach is collaborative involving key researchers at NIST, International SEMATECH, SRC university staff, and integrated circuit (IC) industry personnel. NIST regularly leads and participates in multi-method test studies.

Concurrently, we continue to provide support for thin film calibration standards and methodology developing a mechanism to enable traceability to NIST by suppliers of secondary thin-film reference materials.

Optical methods employed include spectroscopic ellipsometry using an instrument and software developed at NIST to provide structural and optical models. High-resolution x-ray diffraction

techniques and advanced modeling methods have also been developed to a high degree of sophistication in-house. X-ray probes and measurement methods are also used to characterize thin-films and their microstructures.

A new technique, Grazing Incidence X-ray Photoelectron Spectroscopy (GIXPS), was developed and is shown to obtain both thickness and chemical state information of thin films. These measurements are correlated where possible with ellipsometry, AFM, and X-ray reflectometry.

Projects

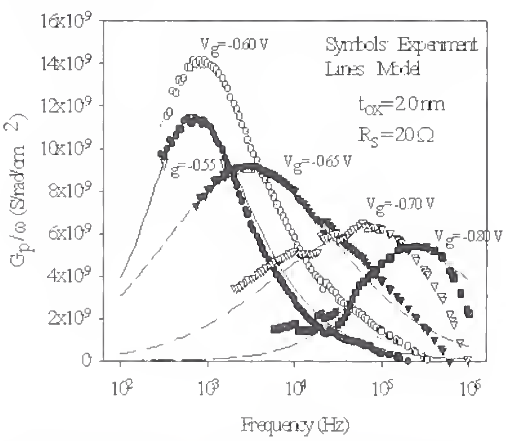
Alternate Gate Dielectric Metrology for CMOS Technology

OU: EEEL

Researchers: Eric Vogel

Funding Sources: NIST OMP (62%)
IST SRD (38%)

- Develop standards, techniques and data for comparison and development of alternate gate dielectrics;
- Obtain device samples and blanket films from other industry and university groups, electrically characterize devices, collaborate with other researchers on analytical characterization;
- Assess, modify and standardize electrical characterization methodologies and data for devices with ultra-thin oxide and oxide-nitride dielectrics;
- Provide standard electrical and reliability measurements, standard electrical data and improved fundamental understanding of electrical properties associated with metal oxide and silicate dielectrics.



Experimental and modeled interface state conductance for a tunneling gate dielectric

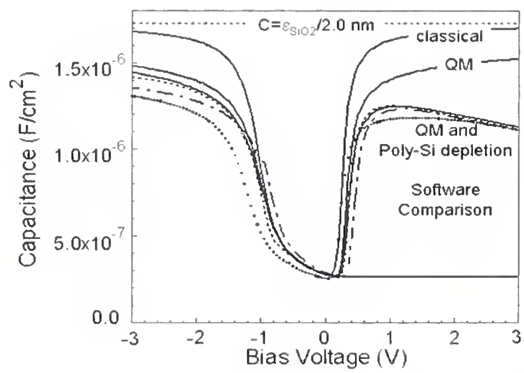
Thin-Film Process Metrology

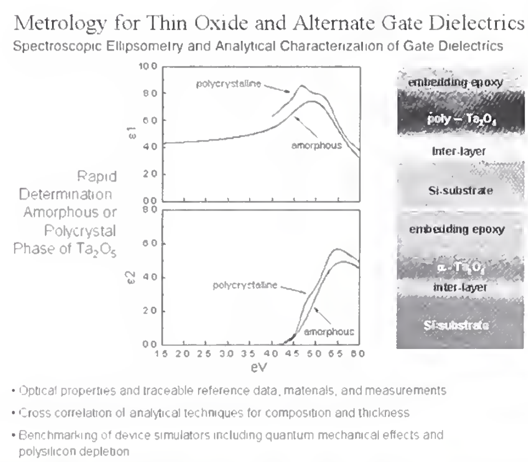
OU: EEEL

Researchers: James R. Ehrstein
Curt A. Richter
Nhan V. Nguyen

Funding Sources: NIST OMP (84%)
NIST: (10%)
Other Agency (6%)

- Focus on relating optical, electrical, and physical measurements of thickness, composition, and interface structure and developing and providing the basis for traceability to NIST for film thickness measurements;
- Identify structural models and develop preferred optical index dispersion models or data for improved ellipsometric analysis of future generation gate dielectric film systems;
- Identify preferred software and use to improve correlation between electrical and ellipsometric methods;
- Transfer to first level commercial suppliers of reference materials traceability to NIST down to 2 nm for oxide films;
- Distribute software to International SEMATECH and collaborating universities for evaluation.





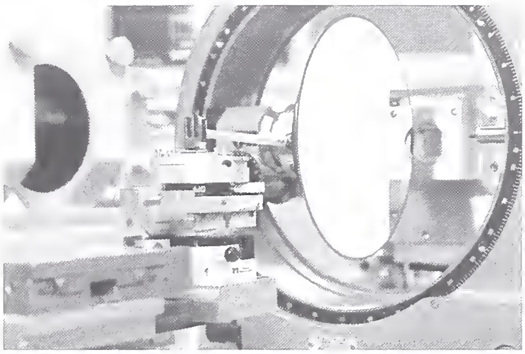
X-Ray Measurement Methods for Characterization of Thin Films and Their Microstructures

OU: PL

Researchers: Richard Deslattes
Richard Matyi

Funding Sources: NIST OMP(20%)
NIST STRS (50%)
Cost Recovery (30%)

- Provide an accurate system of measurements for structural parameters of semiconductor thin-film and multiplayer systems. These techniques need to be non-destructive, non-invasive, and give results robustly connected to the SI.



Detail of Grazing Incidence X-ray Reflectometer

Compositional Metrology for Next Generation Gate Stack Materials

OU: STL
SEL

Researchers: John A Small
Debra Kaiser

Funding Sources: NIST OMP (100%)

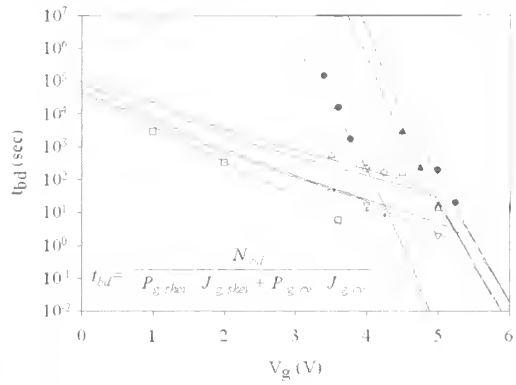
- Develop an approach to fabricate BST thin-film reference standards.

Ultra-Thin Dielectric Reliability Metrology

OU: EEEL

Researchers: John S. Suehle
Eric Vogel

Funding Sources: NIST (100%)

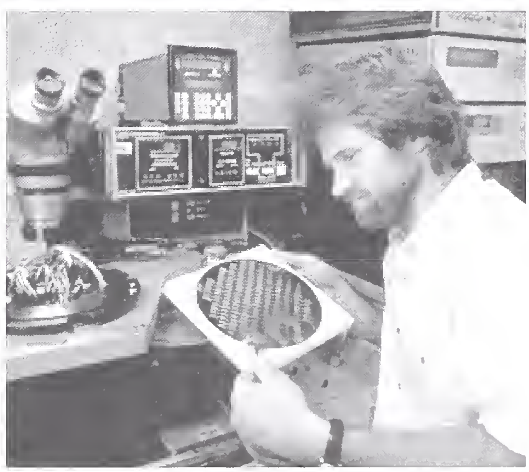


Model and data for combined effects of substrate hot-electron injection and high voltage stress on the lifetime of ultra-thin gate oxides

- Develop and evaluate methods, tools, diagnostic procedures, and physical models for understanding and improving the reliability of ultra-thin SiO_2 and alternate gate dielectrics;

- Develop and evaluate methods, tools, diagnostic procedures, and physical models for understanding and improving the reliability of metal interconnects such as copper;

- Develop new standard voltage stress test for time dependent dielectric breakdown.



Dr. John Suehle preparing to load a sample on wafer prober

Chemical Characterization of Thin Films and Particle Contaminants

OU: CSTL

Researchers: John A. Small, Eric Steel

Funding Sources: NIST OMP (100%)

- Measure sets of well-prepared thin-film insulator samples that will highlight discrepancies between well-established techniques;
- Arrive at corrections that can be applied to each technique to give them absolute sub-nanometer accuracy between 1 nm and 8 nm;
- Develop analysis methods to improve accuracy of analysis for particles less that 100 nm in size;
- Develop analytical standards in support of these measurements;
- Improve beamline optics for GIXPS;
- Develop small angle cleavage technique;
- Improve precision on Si (O, N)x (Sematech providing some samples)

High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

OU: EEL

Researchers: David Wollman, John Martinis, Gene Hilton, Kent Irwin

Funding Sources: NIST OMP (50%), Other Agency (50%)

- Improve x-ray spectrometer system for particle analysis using the unique low-noise, high sensitivity properties of cryogenic electronics;
- Specifically addresses need for improved particle analysis.

Significant Accomplishments

- Demonstration that a Tauc-Lorentz dispersion is the preferred optical model for candidate gate dielectric materials titanium-dioxide and tantalum pentoxide; demonstration of limit for use of a single Tauc-Lorentz oscillator at about 1eV above the optical gap, and demonstration of the ability of spectroscopic ellipsometric characterization to show formation of crystalline phases as a result of processing temperatures.
- Benchmarking-comparisons of five leading university- and industry-developed advanced quantum mechanical modeling programs showed that quantitative differences among the programs in the gate dielectric thickness values they would extract from C-V data are significant compared to levels needed for manufacturing control as outlined in the ITRS.
- A study was conducted investigating the temperature dependence of time-dependent dielectric breakdown in sub-3 nm SiO_2 films. The results indicate that soft and hard breakdown modes exhibit the same thermal acceleration and that the thermal activation energy is observed to decrease for higher gate voltages. The work explains conflicting data trends that have been reported in the literature.
- New work studied the effect of stress interruption on the lifetime of ultra-thin gate oxides. Experiments were conducted to study the effect of periodically interrupting stress to monitor the increase in low-voltage leakage current in ultra-thin oxides, a popular technique for detecting breakdown in ultra-thin oxides. The results show that stress interruption longer than 1s does not affect the defect generation and TDDB life distributions.
- Substrate hot hole injection studies of ultra-thin oxide show that defect generation caused by holes has extremely weak temperature dependence. Furthermore, the results show an oxide can withstand more defects created by holes than created by electrons. The results shed doubt on the current anode hole injection theory for describing oxide breakdown.
- Numerous studies were performed to investigate the reliability of oxide/nitride stacks. Preliminary results indicate the importance of N_2O annealing to reduce the defect generation rate and improve the Weibul slope. The results suggest that an oxide/nitride stack with N_2O anneal has better reliability than an oxide at the same equivalent oxide thickness.
- Initial measurements of the energy distribution of the interface state density of ZrO_2/SiO_2 and ZrO_2/Si_3N_4 are much higher than pure SiO_2. However, the time constant (capture cross section) of these defects are identical to that of SiO_2 suggesting a similar physical nature (i.e. Pb center, silicon dangling bond).
- The hardware, software, and analysis routines for performing 3-level and sinusoidal charge pumping were set up. Defect densities of oxide-nitride stacks were measured and analyzed.

Interconnect and Packaging

Task Goals

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

Customer Needs

The function of interconnect is to distribute signals and to provide power and ground to and among the various components on the integrated circuit. The challenges for $\geq$ 100 nm (pre-2005) include new materials and processes to meet resistivity and low-/high-κ dielectrics. The continuing shrinking of critical dimensions, driving up the impedance of long interconnect lines, and the need to reduce costs, is forcing the rapid introduction of copper with barrier materials and low-κ dielectrics. Beyond 2005, for the $<$ 100 nm technology node, dimensional control and metrology become all the more critical. Solutions beyond copper and low-κ materials must be found.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) connections on circuits with a vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip-chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through Microelectromechanical Systems (MEMS) technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low-environmental-impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.

Technical Strategy

We are providing fundamental measurements on the chemistry of the generic copper plating process, allowing industry to optimize the process for deposition of narrow high-aspect-ratio copper interconnect structures.

In collaboration with industry, we are developing and refining a robust suite of test structures, methods, and diagnostic procedures to evaluate the mechanical and environmental properties and reliability of interconnect and packaging structures. By applying complementary approaches, specific issues are being addressed.

Both miniaturized conventional tensile testers and CMOS-compatible MEMS test structures are being developed to evaluate the mechanical properties of the individual components and the composite structures in interconnect systems.

The conductance and capacitance of transmission line test structures are measured over a wide frequency range to evaluate alternative dielectrics and to permit modeling of the frequency characteristics of interconnect structures.

A high sensitivity capacitance cell has been developed to evaluate the dimensional stability of polymers used in packaging, and a micro-scale thermal conductance method is being developed to permit measurement of the thermal characteristics of packages. Electron-beam Moiré is used to observe deformations in package structures, allowing modeling of micro-scale thermo-hygro-mechanical behavior.

Working with industrial partners, we are developing evaluation techniques for bonding systems, both for wire to chip with emphasis on the new copper/low-κ interconnect, and package to board, with emphasis on lead-free solders.

Projects

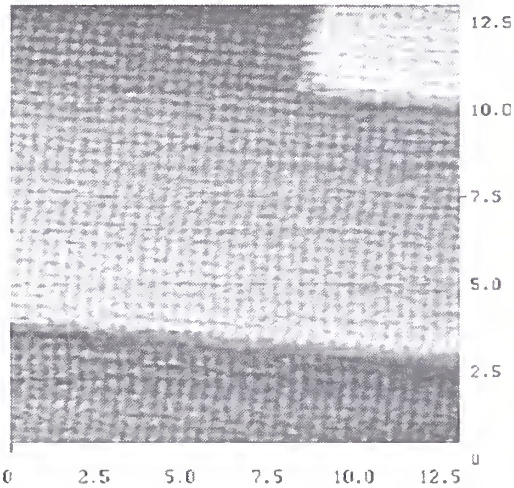
Measurements for Electrodeposited Copper Interconnects

OU: MSEL

Researchers: Gery R. Stafford
Mark Vaudin

Funding Sources: NIST OMP (40%)
NIST STRS (60%)

- Provide better understanding of the mechanism by which organic reagents inhibit copper deposition reaction;
- Understand mechanism of factors controlling copper recrystallization behavior of Cu electrodeposits;
- Determine recrystallization kinetics of copper films as a function of deposition current density and film thickness.



A 13 x 13 nm STM image of ($\sqrt{2}$ x $\sqrt{2}$)R45° chlorine adlattice on Cu(100) at –0.169 V vs. Cu/Cu^+ in 10 mmol/L HCl

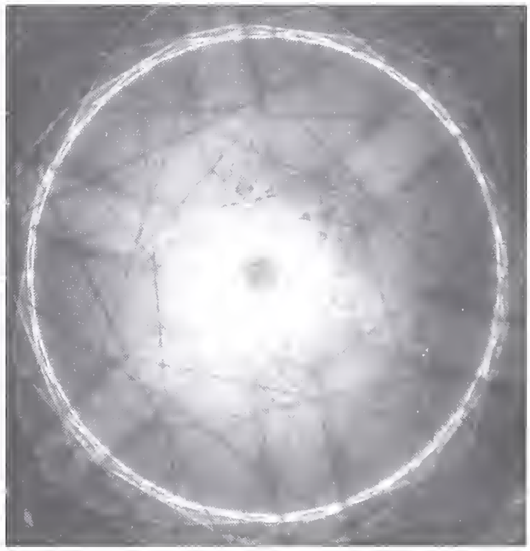
Interconnect Materials and Reliability Metrology

OU: EEEL, MSEL

Researchers: Harry Schafft
David Read
Fred R. Fickett
Robert R. Keller
Chrristine E. Kalnas
John E. Bonevich

Funding Sources: NIST (100%)

- Evaluate test structure designs and test methods for characterizing copper interconnects;
- Design and submit to MOSIS a test structure for tensile testing of metal interconnect layers;
- Measure crystal distortions in copper specimens with extrapolation to interconnect stress and strain states.



TEM electron diffraction pattern of interconnect metallization crystallite

Test Structures for Mechanical Strain Characterization in Integrated Circuit Interconnects

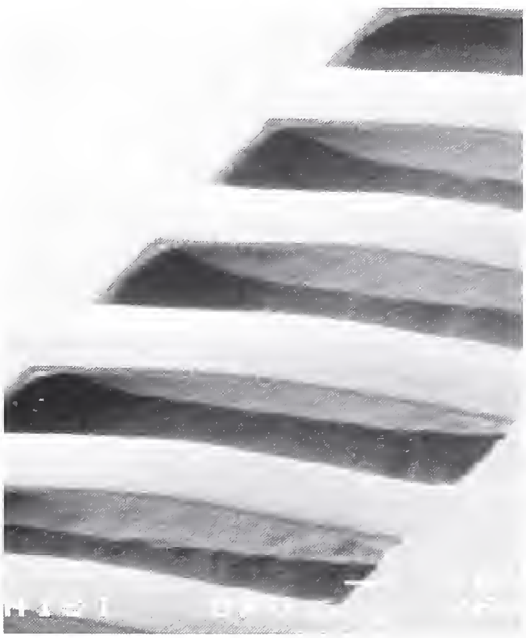
OU: EEEL

Researchers: Michael Gaitan

Funding Sources: NIST OMP (19%)
NIST STRS (57%)
ATP (24%)

- Provide domestic industry with MEMS-based test structures and standardized test methods for characterizing the thermo-electro-mechanical properties of thin films used in integrated circuits suitable for in-line metrology;

- Develop test method for elastic modulus in IC interconnects to derive the mechanical stress of interconnects.



Fixed-fixed beam test structure array for measurement of mechanical strain and interconnects in multilayer structures

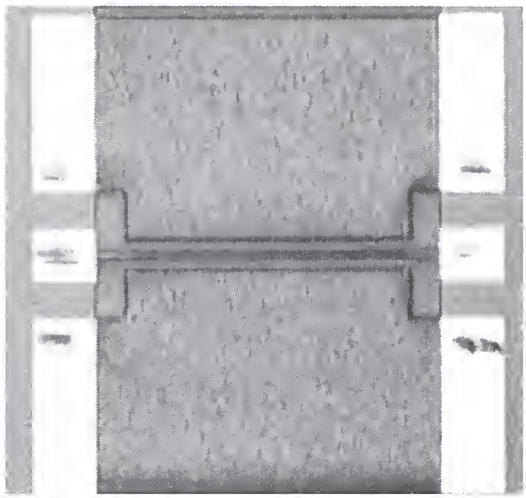
Thin-Film Characterization from Transmission-line measurement

OU: EEEL

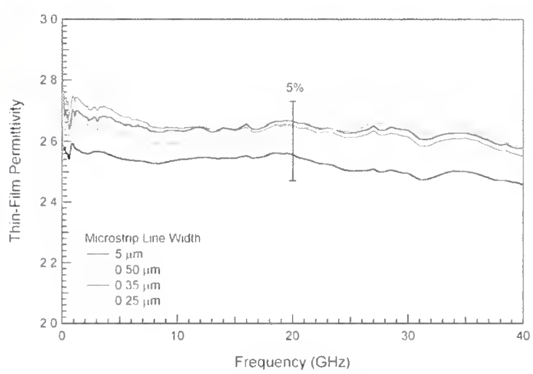
Researchers: Dylan F. Williams
Michael Janezic

Funding Sources: NIST OMP (100%)

- Develop methods to accurately measure the dielectric properties of low-κ thin films from in-situ transmission-line measurements.



Small printed transmission line



Thin-film permittivity from microstrip test structures

Electron Beam Moiré

OU: MSEL

Researchers: Elizabeth Drexler
David Read

Funding Sources: NIST OMP (50%)
NIST STRS (50%)

- Develop and apply Moiré techniques to the measurement of strain and observation at high magnification;
- Assess new method for making Moiré gratings with the goal of sub-25 nm pitches;
- Apply electron beam Moiré to measure displacements at a suspected interfacial flaw identified by thermal microscopy.

Hygrothermal Expansion of Polymer Thin Films

OU: MSEL

Researchers: Chad R. Snyder

Funding Sources: NIST OMP (100%)

- Measure the changes with temperature and humidity of the out-of-plane dimensions on polymer thin films;
- Complete and test new capacitance cell and make available to industrial users.

Capacitance cell

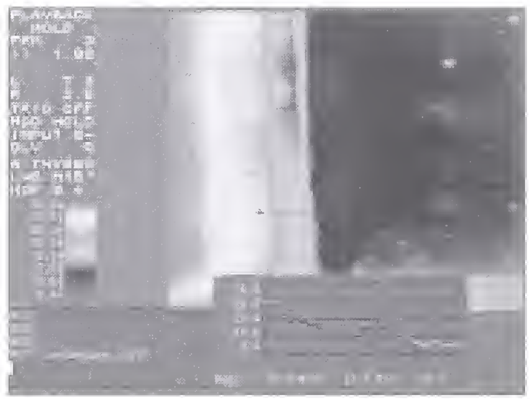
Thermal Conductivity of Microelectronic Structures

OU: MSEL

Researchers: David R. Smith

Funding Sources: NIST OMP (25%)
NIST STRS (75%)

- Demonstrate advanced methods of measurement of thermal effects within packaging structures and their components;
- Develop measurement methods for absolute thermal conductivity of interconnect structures at the micron scale
- Demonstrate quantitative application of infrared microscopy to thermal transport measurement and detection of incipient failure in microelectronic packages.



Thermal image of package structure

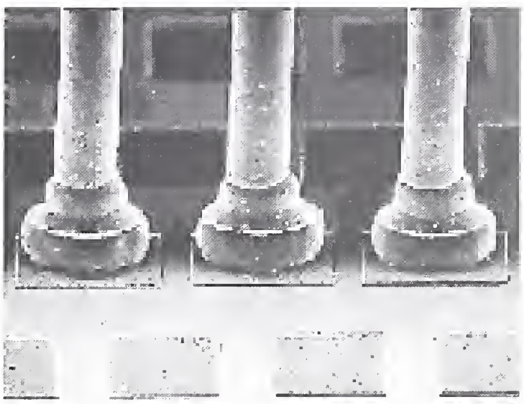
Packaging Studies (Wire Bonding to Cu/Low-κ Semiconductor Devices)

OU: EEEL, MSEL

Researchers: George Harmon
David Kelley
Chris Johnson

Funding Sources: NIST OMP (60%)
NSIT STRS (40%)

- Develop the best/most economical practical bonding surfaces/subsurface support structures and techniques for wire bonding to advanced semiconductor devices with Cu metallization;
- Resolve diffusion issues that relate to these interfaces;
- Determine diffusion coefficients of Cu into Au using metal films deposited in the same manner as on Cu-conductor chips and evaluate the results with actual wire bonding experts.



Scanning electron micrograph of tine-wire wire bonds

Solderability Measurements for Microelectronics

OU: MSEL

Researchers: Frank Gayle
Gery R. Stafford

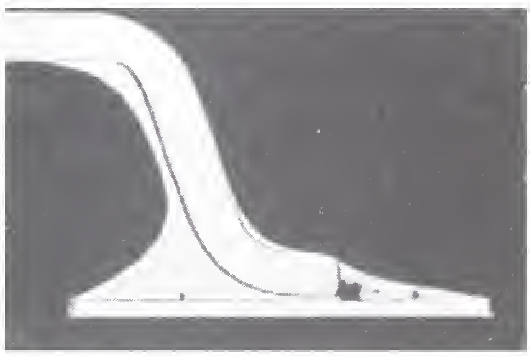
Funding Sources: NIST OMP (100%)

- Improve solderability test methods, including new lead-free solders;
- Facilitate high-temperature-fatigue-resistant-solder consortium.

Significant Accomplishments

Filed a patent on (NIST Docket #00-018US) entitled: **"Inorganic Non-Metallic, Wire Bondable Top Surface Coating For Use In Wire Bonding To Copper Metallization On Semiconductor Chips "**

Researchers successfully completed the Hygrothermal Expansion of Polymer Thin Films project. Drawings of the capacitance cell are available for transfer to the industry.



Cross-section of soldered lead

Wafer Characterization and Process Metrology

Task Goals

Device scaling has been the primary means by which the semiconductor industry has achieved the unprecedented gains in productivity and performance quantified by Moore's Law. With the replacement of the traditional silicon dioxide/ polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled accuracy, robustness and ease of use.

Customer Needs

Continued reduction in transistor dimensions demand tighter control of silicon substrate flatness, dopant and oxygen content, and surface ion and particle contamination. Tighter process control is required to fabricate the intricate transistor, passive component and interconnect structures.

Technical Strategy

A broad suite of wafer characterization metrology tools and methods are being developed and used to address industry needs for wafer flatness, particle contamination and identification, and doping level monitoring. A wide range of process metrology development, fundamental properties, measurement services, and reference materials are under development. Both destructive and nondestructive techniques are being investigated, with emphasis on the later for in-line and at-line metrology.

A variety of optical techniques are being developed to provide metrology for both wafer geometry and oxygen content. The goal is to provide full wafer characterization non-destructively.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters are being measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties; a low water vapor pressure calibration facility has been developed and is being used by industry for calibration of water vapor sensors.

A wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture. A number of projects are addressing contact-less thermometry, particle formation, and plasma diagnostics with an emphasis on real time control.

Detection and accurate sizing of particle contamination continues to challenge semiconductor manufacturing. Methods for rapid detection as well as polystyrene latex spheres for calibration standards are under development.

Projects

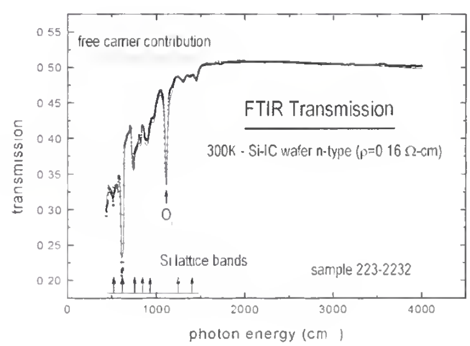
FTIR Methodology for Quantifying Oxygen in Heavily Doped Silicon

OU: EEEL, CSTL

Researchers: Deane Chandler-Horowitz
James E. Maslar

Funding Sources: NIST OMP (100%)

- Develop FTIR methodology for measuring interstitial oxygen in conducting silicon wafers.



Wafer and Chuck Flatness and Thickness

OU: MEL

Researchers: Christopher Evans
Angela Davies
E. Clayton Teague

Funding Sources: NIST OMP (100%)

- Develop full aperture interferometric methods to evaluate important wafer characteristics such as flatness, thickness, thickness variation, and bow.

Preliminary evaluation of high spatial frequency noise of 0.037 nm rms

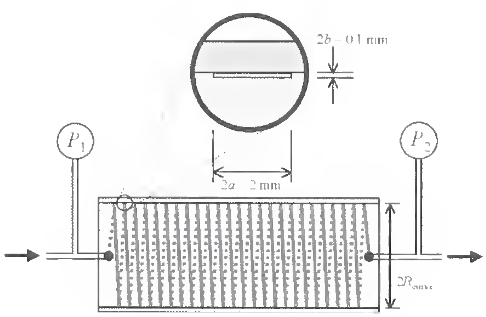
Fundamental Process Control Metrology for Gases

OU: CSTL

Researchers: Robert Berg

Funding Sources: NIST OMP (100%)

- Develop primary flow standards in the flow range for 10^{-7} mol/s to 10^{-3} mol/s and transfer these capabilities to the semiconductor industry;
- Support process control with improved RGA or PPA and in-situ RGA and PPA calibration techniques.



Laminar flow element (S.A. Tison & L. Berndt, 1997)

Low Concentration Humidity Standards

OU: CSTL

Researchers: Joseph T. Hodges
Gregory E. Scace

Funding Sources: NIST OMP (75%)
Other Agency (25%)

- Establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{-13}$ molecules/cm^3);
- Support the development and application of commercial humidity sensors for gas purity measurements.

Details of the Low Frost Point Generator (LFPG)

Plasma Process Measurements

OU: EEEL, CSTL, PL

Researchers: James K. Olthoff
Mark Sobolewsski
Kristen Steffens
Eric Benk
L. Christophorou

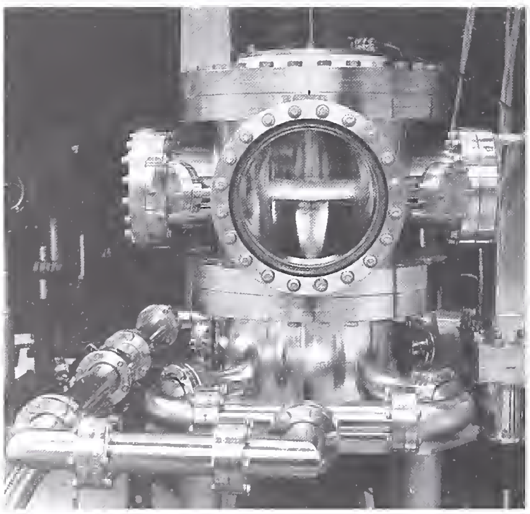
Funding Sources: NIST OMP (65%)
NIST ATP (5%)
NIST SRD (5%)
NIST STRS (15%)
Other Agency (10%)

- Develop diagnostic techniques and physical understanding of low temperature discharges necessary for real time control and predictive modeling of plasma etch and deposition processes;

- Develop rf-based ion-flux and ion energy measurement technology, transfer the technology to industrial partners, and assess its utility in commercial plasma processes;

- Measure composition and energies of ion fluxes generated in reactive plasmas exposed to semiconductor wafers;

- Complete development of optical tomography as a plasma uniformity diagnostic and demonstrate performance on a commercial etching reactor.



Gaseous Electronic Conference (GEC) cell

Metrology for Contamination–Free manufacturing

OU: CSTL

Researchers: Ronald W. Davis
Donald R. Burgess

Funding Sources: NIST OMP (100%)

- Acquire an improved understanding of the physics and chemistry of gas-phase-generated microcontaminants in thermal CVD reactors;

- Develop a predictive capability for this phenomenon that can be utilized to guide process parameter selection and develop microcontamination standards;

- Develop experimentally validated numerical models for microcontaminant formation, growth and transport in rotating disk CVD reactors.

Temperature Sensing for Rapid Thermal Processing

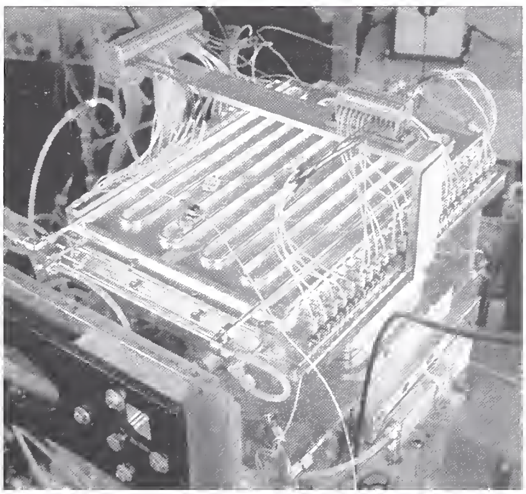
OU: PL, CSTL

Researchers: Benjamin K. Tsai, David P. DeWitt, Kenneth G. Kreider, Christopher W. Meyer

Funding Sources: NIST OMP (65%), NIST STRS (35%)

- Develop technologies required to enable measurement of RTP wafer absolute temperatures with uncertainties of 2 °C at 1000 °C;

- Develop a calibration wafer using thin-film thermocouple technology, establish procedures for in-tool calibration of radiation thermometers, and collaborate with the semiconductor industry in implementing new methods for traceable temperature measurement.



Rapid thermal processing thermometry test bed

Thin-film thermocouple test wafer

Particle Measurements in Support of the Semiconductor Industry

OU: BFRL

Researchers: George W. Mulholland, William Pitts

Funding Sources: NIST OMP (100%)

- Develop a facility for accurately measuring particle size and concentration and for depositing monosize particles on calibration artifacts with the goal of quantifying 60 nm by 2001 and 33 nm by 2006.

Optical Scattering for Wafer Surface Metrology

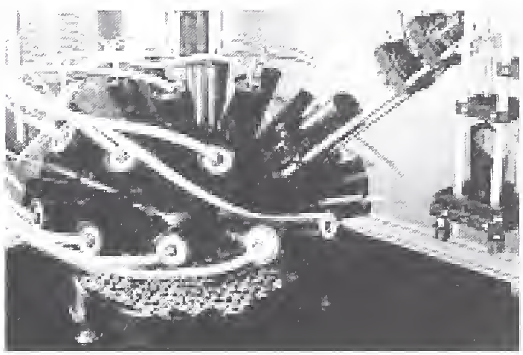
OU: PL

Researcher: Thomas A. Germer

Funding Sources: NIST OMP (60%), NIST STRS (40%)

- Improve understanding of the behavior of light scattering from defects, contaminants, and roughness needed to improve optical inspection of wafer surfaces;

- Develop technique of ellipsometry for defect characterization.



Optical scatterometer system

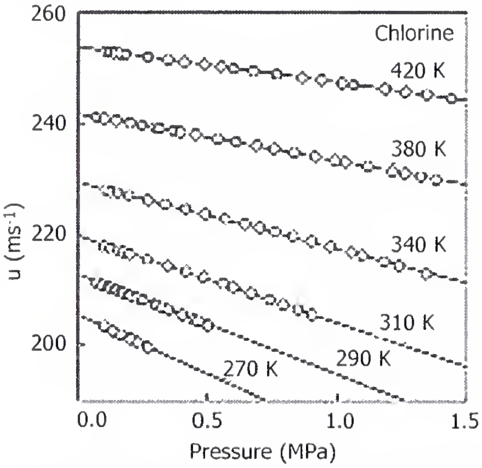
Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

OU: CSTL

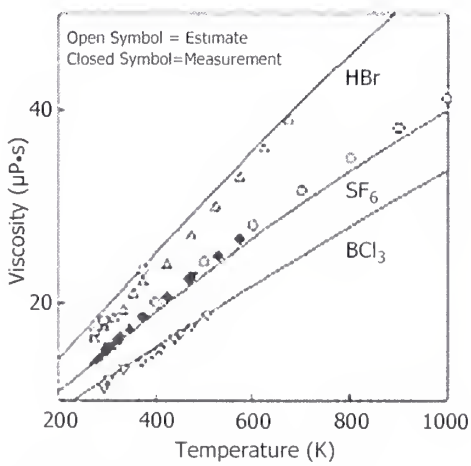
Researchers: Michael Moldover
John Hurley

Funding Source: NIST OMP (100%)

- Measure the thermophysical properties of process gases, surrogate gases, and binary mixtures of process and carrier gases;
- Disseminate the results as a data base providing the heat capacity, thermal conductivity, viscosity and the pressure-density-temperature relation for the process gases and diffusion coefficients for the gas mixtures.



Representative data. NIST speed-of-light data for chlorine as a function of pressure on various isotherms



Viscosity of gases at low density

Significant Accomplishments

- Measurement of the thermophysical properties of WF_6 has been completed. The thermophysical properties of WF_6, HBr, and BCl_3, important semiconductor manufacturing gases, have been published. These data are fundamental for calibrating mass flow controllers for these gases;
- A database of thermophysical properties of semiconductor process gases has been constructed and made available to the entire semiconductor community at http://properties.nist.gov/semiprop;
- Extended the light scattering analysis technique to detection of metallic particles, critically important in semiconductor manufacturing. Used light scattering to determine roughness scattering from CaF_2 materials being considered for deep ultraviolet lenses at 193 nm and 157 nm.

Lithography

Task Goals

As device dimensions continue to shrink, the wavelength of the radiation used by the lithography exposure tools has moved into the deep ultraviolet (DUV) spectrum. Currently exposure tools operating at 193 nm are being introduced, and exposure tools operating at 157 nm are in development. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV.

Customer Needs

The semiconductor industry needs materials with well-characterized optical properties for use as optics and masks in the DUV region of the spectrum. Accurate, reliable radiometers suitable for use as wafer-plane dosimeters are needed both in the DUV and EUV. High accuracy surface measuring capability is needed both for EUV mask and optics characterization. The reflectivity of the EUV mirrors (some as large as 400 mm in diameter) must be accurately measured as a function of wavelength (near 13.4 nm), angle of incidence, and position.

Technical Strategy

We have established capability for highly accurate measurements in the region surrounding 157 nm of the index of refraction, dispersion, and stress-induced birefringence of the materials to be used for the DUV optics and mask reticles at this wavelength. It is also necessary to be able to accurately measure the index of refraction for both the N_2 and Ar used as purge gasses in the 157 nm DUV steppers.

In addition to the measurement capability, it is necessary to develop DUV transfer standards to assist the equipment vendors and process engineers in qualifying the equipment and processes used in this wavelength area.

Photodetectors and energy meters that are radiation resistant are crucial for use with the DUV excimer lasers.

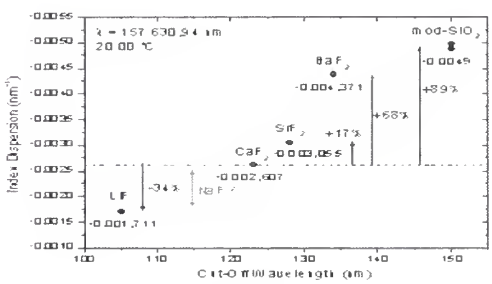
We will provide leading edge metrology for the development and characterization of optical components and detectors to be used in EUV lithography.

Projects

Metrology for Deep Ultraviolet Lithography

OU:	PL, EEEL
Researchers:	John H. Burnett Rajeev Gupta Chris Cromer Marla Dowell Richard Jones Holger Laabs Darryl Keenan
Funding Sources:	NIST OMP (50%) NIST STRS (50%)

- Measure accurately (≈ ppm) the index of refraction as a function of temperature, dispersion, transmission, and stress-induced birefringence of CaF_2 and other DUV transmitting materials in the region near 157 nm;
- Establish calibration services for laser power and energy meters and develop transfer standards for pulsed laser radiometry of DUV excimer lasers;
- Study 157 nm radiation damage mechanisms of optics and detectors.



Dispersion of VUV Materials

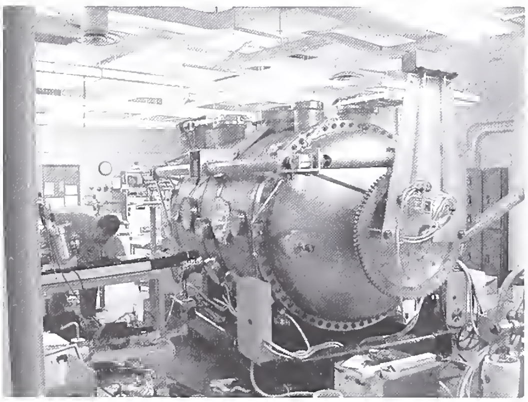
Metrology for EUV Lithography

OU: MEL, PL

Researchers: Angela Davies
Chris Evans
Tom Lucatorto
Charles Tarrio
Keith Lykke

Funding Sources: NIST OMP (20%)
NIST STRS (80%)

- Commission "XCALIBIR," a unique NIST-designed phase-measuring interferometer for nanometer-level optical figure measurement that will augment the present state-of-the-art figure measuring capability and will be used for wafer flatness and mask flatness characterization;
- Commission the large reflectometer that is part of the NIST/DARPA EUV Optics Characterization Facility. (This reflectometer is the only one in the world capable of providing a point-by-point map of the reflectivity for the large mirrors to be used in EUV steppers such as the ETS Alpha tool presently being assembled by the EUV-LLC.);
- Develop a calibration capability for the detectors to be used as EUV wafer-plane dosimeters.



EUV reflectometer for large lenses used in EUV lithography tool

Significant Accomplishments

- With funding support from SEMATECH and OMP, completed development of a new DUV primary standard calorimeter for measurement of 193 nm excimer laser pulse energy. Established 193 nm excimer laser power and energy meter calibration services with an expanded uncertainty of ≈ 1 %.;
- Established a measurement system for the transmittance of optical materials (e.g., fused silica and calcium fluoride) using a 193 nm excimer laser. Measurements are performed in a nitrogen gas environment with an uncertainty of < 1 %, and are available to customers as a special test;
- Completed survey of 157 nm index and dispersion of latest grades of CaF_2 from all major suppliers, establishing a supplier index variation of about 10 ppm. Determined that BaF_2 satisfies the criteria for second index material after completing a survey of 157 nm index and dispersion of all candidate second index materials to be used with the CaF_2 for optics achromatization. The survey for second index material included BaF_2, SrF_2, and LiF;
- Completed initial measurements of the characterization and degradation of photodiodes after irradiation from an excimer source at 157 nm;
- Completed the measurements of high accuracy transmission measurements of transmissive materials in the spectral range from 120 nm to 300 nm;
- Established a measurement system for the spatial characterization of excimer laser beams, which includes the capability for performing measurements of irradiance profiles, beam divergence, M^2 values, spatial uniformity, and spatial irradiance correlations;
- Designed and constructed a measurement system for energy density, or dose, measurements using 193 nm excimer laser. Progressing on schedule to complete characterization of this system by the end of calendar year 2001;
- Completed XCALIBIR installation and made first measurements as part of the process of commissioning.

Modeling, Design, and Test

Task Goals

Device scaling to atomic dimensions and integration of components on single chips exceeding a billion active components requires new concepts in modeling of processes, circuit performance, and thermal management. Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The overall task is to develop modeling and test methodologies to address these new requirements.

Customer Needs

The industry needs very efficient and reliable simulation methods as device structures and packages continue to rapidly evolve. Conventional methods are no longer suitable and simulators must include quantum mechanical physics. Researchers at NIST recognize that the most efficient and appropriate way to approach the challenge is to work in concert with an industry consortium (Semiconductor Research Corporation), and the National Science Foundation bringing together the top people in workshops and working groups.

Accurate at-speed test methodology of digital integrated circuits is also a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial.

Technical Strategy

With the challenges facing designers and the rising costs of development, it is extremely important to develop accurate testing, modeling and simulation strategies. Keeping pace with the technology and serving the needs of the industry involve more than basic measurements.

Benchmarking semiconductor device simulation tools that include quantum mechanical effects are important facets of the overall strategy. These software tools include MEDICI, UTQuant, NCSU code, and NEMO, all widely used in industry. The NIST/IEEE Model Validation Working Group continues the development of the infrastructure necessary for validating the performance of compact models.

The thermal performance of a system can be accurately simulated through the application of the NIST electro-thermal network simulation methodology. Methodologies are being developed to validate the performance and accuracy of compact thermal models that support the shrinking device architecture.

The development of calibration artifacts and procedures are also very important. Specifically, calibration artifacts in the form of custom integrated circuits containing special test structures and precisely known high-frequency voltages and circuits will be devised. Calibration procedures applied to miniature AFM probes will test both the intermittent and non-contact modes of scanning capacitance microscopy.

Time-Domain Reflectometry (TDR) will be used to characterize a number of multichip-module and discrete package interconnect systems. The calibration approaches will be verified using the sinusoidal signals, waveform measurement capability will be developed as will pulsed versions for calibration of the time-domain measurement systems.

Projects

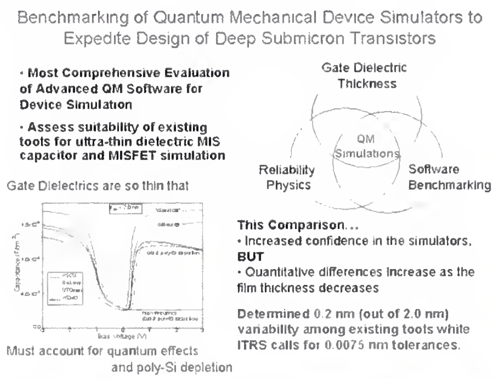
Metrology for Simulation and Computer-Aided Design

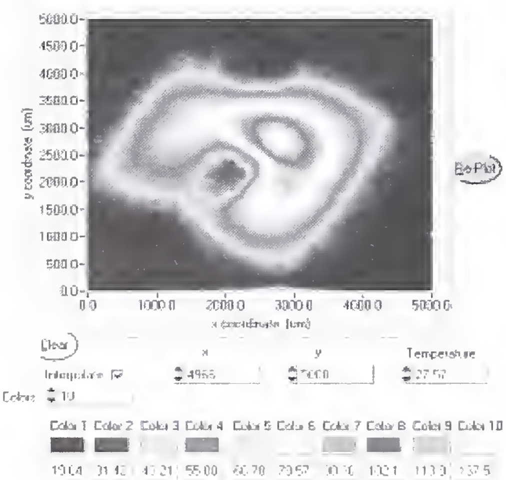
OU: EEEL

Researcher: Allen R. Hefner, Jr.

Funding Sources: NIST OMP (47%)
NIST STRS (36%)
NIST ATP (15%)
Other Agency (2%)

- Facilitate efficient and reliable application of semiconductor CAD tools by development of industry infrastructure for establishing model accuracy, methods, and for simulator model verification and benchmarking;
- Develop metrology for providing model data and model parameter extraction techniques sequences;
- Develop models and techniques necessary for advanced device process, package, and system simulation.





Formation of Dynamic Hot Spot

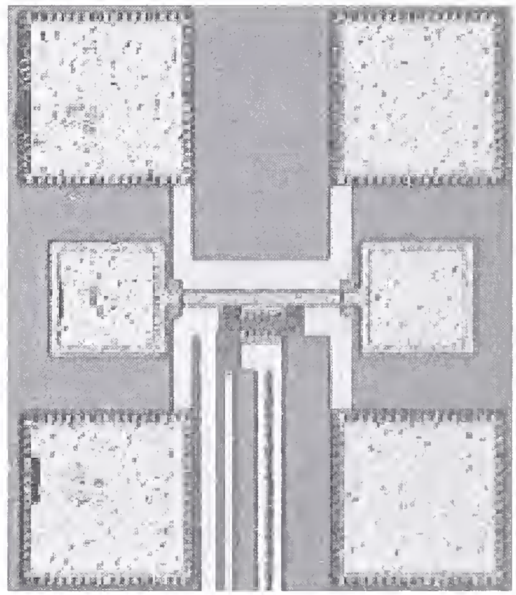
At-Speed Test of Digital Integrated Circuits

OU: EEEL

Researchers: Dylan Williams
John Moreland
Joseph J. Kopanksi

Funding Sources: NIST OMP (100%)

- Develop metrology for the at-speed test of digital integrated circuits through the resolution of the essential metrology issues;
- Apply results to atomic force microscopes modified to precisely position field probes above the surface of the integrated circuit.



Integrated circuit test structure for high-speed testing development

Significant Accomplishments

- A new high speed transient thermal imaging system was developed that provides the capability to measure the transient temperature distributions on the surface of a silicon chip with one-microsecond time, and fifteen-micrometer spatial resolution. The system uses virtual instrument graphical user interface software that controls an infrared thermal microscope, translation stages, digitizing oscilloscope, and a device test fixture temperature controller. The new system is more than four orders of magnitude faster than conventional infrared thermal imaging systems. The higher speed enables the observation of semiconductor device dynamic failure events and enables the localization of small heat sources before the heat has time to diffuse to surrounding areas;

- Researchers in the Semiconductor Electronics Division (SED) initiated a study to compare, for the first time, quantum mechanical simulators and analysis software suites that are critical to the continued shrinking of silicon complementary metal oxide semiconductor (CMOS) transistor structures. The SED's Dr. Curt Richter, in collaboration with Drs. Allen Hefner and Eric Vogel, presented invited summaries of these findings to the SEMATECH Gate Stack Engineering Working Group and the International Metrology Council. A paper was also published in the IEEE Electron Device Letters. As a result of Dr. Richter's presentation on quantum mechanical (QM) Benchmarking, Professor John Hauser (NCSU), who has produced one of the more widely used QM codes, changed his simulation code. Professor Hauser contacted Dr. Richter via e-mail, stating, "Your presentation last week prompted me to take another look at how I have been modeling the polysilicon depletion problem ... I have gone back and changed slightly my first order model for polysilicon depletion." As an additional result of Dr. Richter's presentation, the Lucent Technologies' electrical characterization team in Orlando plans to acquire and use John Hauser's revised code; the code adjustment is already propagating into industry's metrology practices.

Appendix A: Index of Researchers

Appendix B: NIST-Wide OMP Managed Projects

National Semiconductor Metrology Program FY2001

Building and Fire Research Laboratory (BFRL)

- Particle Measurements in Support of the Semiconductor Industry 865

Chemical Science and Technology Laboratory (CSTL)

- Thin-Film Profile Measurement Methods and Reference Materials 837
- Chemical Characterization of Thin Films and Particle Contaminants 837
- Fundamental Process Control Metrology for Gases 836
- Low Concentration Humidity Standards 836
- Plasma & CVD Process Measurements 836 (with EEEL 811 & PL 842)*
- Metrology for Contamination-Free Manufacturing 836
- Temperature Measurement for Rapid Thermal Processing 836 (with PL 844)*
- Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers 836

Electronics and Electrical Engineering Laboratory (EEEL)

- Linewidth and Overlay Standards for Nanometer Metrology 812
- Scanning Probe Microscopy for Dopant Profiling 812
- Alternate Gate Dielectric Metrology for CMOS Technology 812
- Thin Film Process Metrology 812
- Ultra-Thin Dielectric Reliability Metrology 812
- Test Structures for Mechanical Strain Characterization in IC Interconnects 812
- High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis 814
- Interconnect Materials and Reliability Metrology 812 (with MSEL 853)*
- Plasma & CVD Process Measurements 811(with CSTL 836 & PL842)*
- Deep Ultraviolet Laser Metrology for Semiconductor Photolithography 815
- Metrology for Simulation and Computer-Aided Design 812
- Thin-Film Characterization for Transmission-line Measurement 813
- At-Speed Test of Digital Integrated Circuits 813
- Packaging Studies (Wire Bonding to Cu/Low κ Semiconductor Devices) 812 (with MSEL)* 855
- Metrology for Deep Ultraviolet Lithography 815 (with PL 842 844)*

Manufacturing Engineering Laboratory (MEL)

- Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques 821
- Nanometer-Scale Dimensional Metrology with Atomic Force Microscopy 821
- Scanning Electron Microscope Dimensional Metrology 821
- Model-Based Linewidth Metrology 821
- High Accuracy Tow-Dimensional Metrology 821
- Atom-Based Dimensional metrology 821
- Optical Overlay and CD Metrology 821
- Wafer and Chuck Flatness and Thickness 822
- Metrology for EUV Lithography 822 (with PL 841)*

Materials Science and Engineering Laboratory (MSEL)

- Experimental Micromechanics by e-Beam Moiré 853
- Interconnect Materials and Reliability Metrology 853 (with EEEL 812)*
- Thermal Conductivity of Microelectronic Structures 853
- Solderability Measurements for Microelectronics 855
- Measurements for Electrodeposited Copper Interconnects 855
- Packaging Studies (Wire Bonding to Cu/Low κ Semiconductor Devices) 855 (with EEEL 812)*

Physics Laboratory (PL)

- Plasma Process measurements 842 (with CSTL 836 & EEEL 811)*
- Temperature Measurement for Rapid Thermal Processing 844 (with CSTL 836)*
- Optical Scattering for Wafer Surface Metrology 844
- Metrology for Deep Ultraviolet Lithography 842 844 (with EEEL 811)*
- Metrology for EUV Lithography 841 (with MEL 822)*

Appendix C:
Key to Funding Sources

NIST OMP:
NIST Office of Microelectronic Programs

NIST STRS:
NIST Scientific and Technical Research and Services

NIST SRMP:
NIST Standard Reference Material Program

NIST SRD:
NIST Standard Reference Data

NIST ATP:
NIST Advanced Technology Program

OTHER Agency:
The designation of "Other Agency" may include, but is not limited to, International SEMATECH, DARPA/ARPA, and the National Science Foundation.

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